ABSTRACT

A process for forming a DRAM stacked capacitor structure with increased surface area, has been developed. The process features forming lateral grooves in the sides of a polysilicon storage node structure, during a dry etching procedure used to define the storage node structure. The grooves are selectively, and laterally formed in ion implanted veins, which in turn had been placed at various depths in an intrinsic polysilicon layer via a series of ion implantation steps, each performed at a specific implant energy. An isotopic component of the storage node structure, defining dry etch procedure, selectively etches the highly doped, ion implanted veins at a greater rate than the non-ion implanted regions of polysilicon, located between the ion implanted veins, resulting in a necked profile, storage node structure, featuring increased surface area as a result of the formation of the lateral grooves.